Qualification of low-K 90nm Technology Die with Pb-free Bumps on a Build-up Laminate Package (PBGA) with Pb-free Assembly Processes

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Abstract

Flip-chip packages have become the preferred solution for high-performance ASIC and microprocessor devices. Typically these are packaged in organic or ceramic Ball Grid Array (BGA) connections. Recently, there has been a significant focus on Pb-free packages to meet European Union mandated RoHS guidelines with exemptions allowed for server and other networking hardware. Towards this goal, IBM has been actively developing and qualifying Pb-free and Pb-reduced packages that cover the range of advanced semiconductor technologies such as 130nm and 90nm ground rules. In addition, for device performance reasons, the BEOL wiring layers on the high-performance 90nm wafers also require low-K dielectric materials. Finally, due to tighter wiring ground rules and faster device performance requirements, the build-up laminate packages require thin-core (400 micron) and advanced wiring pitch in the build-up layers. IBM has partnered with Amkor Technology to qualify both 130nm and 90 nm devices with Amkor developed Pb-free bumps using large die and build-up laminates. The die size used is ~15mm and the laminate qualified is 42.5mm with 1mm pitch Pb-free BGA. The bump pitch is 200micron.

In this paper, we will summarize the Sn/Ag Pb-free plated bumps that have been qualified for low-K 90nm technology on thin-core build-up laminates. Optimizations required for underfill material compatible with Pb-free bumps and low-K die will be reviewed. Finally, high speed devices generate a significant amount of power, and an optimum thermal solution for FC-PBGA package is essential. Summary of package-level thermal performance is presented.

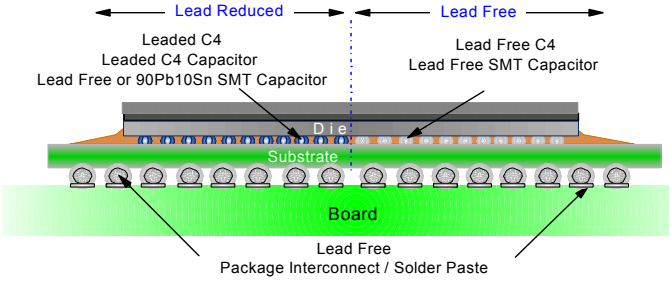
I. Introduction

Pb-based solders have been used as the primary interconnection material for flip-chip, SMT and BGA attach to both ceramic and organic chip carriers. Recently, there has been a worldwide move to develop and implement Pb-free solders in microelectronics packages such as FC-BGA, and also for card assembly. The primary drive for Pb elimination is environmental: Pb is toxic and there are increasing concerns of Pb leaching into ground water from electronic consumer products which are typically disposed of in landfills. The European Union (EU) Directive 2002/95/EC pertaining to the "restriction of the use of certain hazardous substances in electrical and electronic equipment" (usually referred to as the "RoHS Directive") directs the EU member states to pass laws embodying the Directive's requirements which include the reduction and/or elimination (to a given threshold value) of Pb-based solders for equipment put on the market starting July, 2006. The RoHS Directive restricts lead, mercury, cadmium, hexavalent chromium, PBB and PBDE in homogeneous materials to maximum threshold values specified in an amendment to the Annex of the Directive. The Directive Annex and amendments include two key exemptions relevant to flip chip packages:

- Lead in high melting temperature solders (i.e. tin-lead solder alloys containing more than 85% lead)
- Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip-chip packages.

Consistent with RoHS guidelines, IBM has defined two flip-chip package options as explained below, and shown schematically in Fig 1.

- Lead reduced – Leaded C4 (bump) with lead free package (note: for RoHS compatibility, SMT capacitors require joining with lead free solder or exempted >85%Pb alloy)
- Lead free – Lead free bump and package *(Please see note under reference regarding IBM's definitions of Pb-free and Pb-reduced packages)*



C4 = Controlled Collapsed Chip Connection, widely known in the industry as "bump".

Fig. 1: Schematic of IBM's Pb-reduced and Pb-free FC-PBGA

In line with both industry trend and RoHS requirements, IBM has been developing and qualifying both Pb-reduced and Pb-free packages (1). In addition to Pb-free bumping and package requirements, the technology drivers for devices are for low-K dielectrics, and Pb-free packages have to be qualified with low-K devices (2,3). In the following section, device attributes for various technology, along with Pb-free bump and organic chip carrier structures are reviewed.

II. Device, Pb-free Bump and Package Attributes

The device technology roadmap for IBM ASICs menu is shown in Table I. As can be clearly seen, the driving force in the near-future is for higher speed, circuit density, and use of low-k dielectric wiring layers. In addition to the higher circuit

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density, future devices require a reduction in C4 or bump pitch to 200 micron for 90nm technology followed by 150um pitch in 65nm technology. Consistent with the device roadmap and RoHS guidelines, IBM has developed and qualified both Pb-reduced and and Pb-free packages for FC-PBGA.

The key attributes of RoHS compatible FC-PBGA packages for 130 and 90nm devices are shown in Table II. Both Pb-reduced and Pb-based packages have been available for 130nm node, and are not shown in this Table. The Pb-free bumps are plated Sn/Ag bumps with a range of Ag in the 2-3 wt%. IBM has partnered with Amkor to qualify the plated bumping technology for FC-PBGA products for both Pb-reduced (high-Pb C4) and Pb-free bumps. In the technology qualification reviewed in this paper, bond and assembly was carried out at an Amkor facility.

Si Technology (ASIC)			
Process Technology (nm)	130	90	65
Vdd (V)	1.2/1.6	1.0/1.2	1.0
Gate Delay (ps)	15.2-19.1	6.9-15.6	6.1-9.9
Power Dissipation (µW/MHz/gate)	0.009	0.006	0.0045
Raw Circuit Density (Kgates/mm2)	175	310	615
Total Metal Level	6	6-8	8-9
Dielectric	FTEOS	Low K CVD	Low K CVD
Minimum Bump Pitch (µm)	225	200	150

Table I: Key parameters for present and future ASICs devices.

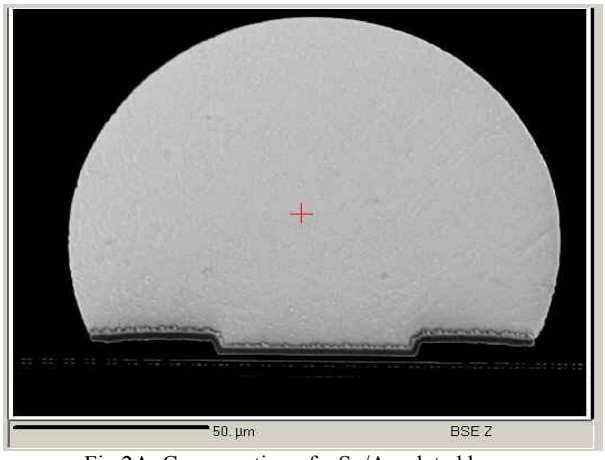

Fig 2A. Cross-section of a Sn/Ag plated bump

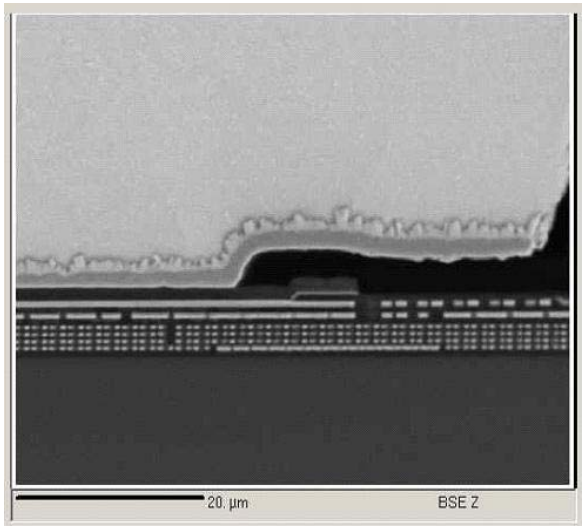

Fig. 2B. Higher magnification showing the Ni barrier layer in UBM (grey layer)

Details of Amkor/Unitive plated bumping technology can be found in Ref. 4, and results of a Pb-free qualification using Sn/Ag plated bumps with a non-lowK device on a laminate package can be found in Ref. 5. The bump structure consists of a sputtered seed layer for adhesion to die passivation followed by a thin Cu layer. The seed layer is used to plate a 2-3 micron Ni layer and the solder through a patterned thick-film resist. A polyimide passivation layer is utilized in IBM wafers with a via to connect the UBM/bump to device wiring layers. For 90nm technology, a photosensitive polyimide passivation is used. A cross-section of a Pb-free bump is shown in Fig 2A, with a higher magnification of the under-bump metallurgy or UBM shown in Fig 2B.

Si Technology	130 nm Lead Free	90nm Lead Reduced	90nm Lead Free
Max Carrier size (*)	42.5mm	42.5mm	42.5mm
Carrier Build-Up Layers	Up To 4	Up To 4	Up To 4
Core Thickness	Thick core (800um)	Thin core (400um)	Thin core (400um)
Lid Type	DLA or with lid	2PL or 1PL	2PL
Max Die Size (mm) (*)	14.7 X 14.7	14.7 x 14.7	14.7 x 14.7
Bump Pitch (um)	225	200	200
Bump Solder	Plated Sn/Ag	Plated Pb/Sn (Sn : 3-5%)	Plated Sn/Ag
LICC/MTLIC Assembly	SAC solder	SAC solder	SAC solder
BGA Alloy	Sn3.0Ag0.5Cu	Sn3.0Ag0.5Cu	Sn3.0Ag0.5Cu
MSL	MSL 3, 245C with 260C rework support	MSL 3, 245C with 260C rework support	MSL 3, 245C with 260C rework support
Technology Qualification Status	Complete	Complete	Complete

Table II: FC-PBGA package attributes for Pb-reduced and Pb-free bump and assembly.

(*) IBM is expanding the qualified application space to 55mm laminate space with a die size of approximately 19mm.

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The testsite used for low-K device with Pb-free bumps had four layers of low-K wiring with fine wire ground rules followed by three layers of FTEOS wiring with fat wire ground rules. The devices used in the qualification were made on 300mm wafers by IBM followed by bumping by Amkor. The following section has details about the laminate package and Pb-free bond and assembly processes.

The need for a thin-core build-up laminate with 90nm technology was driven by both electrical performance and higher wirability requirements as listed below:

1) Thin-core laminates allow lower PTH (plated-through hole) pitch of 250 micron compared to 500 micron in thick core. Denser PTH enables better wirability in the bottom build-up layers of the laminate package.

2) Loop inductance is 2x lower in a thin-core package comapred to thick-core. In addition, ~ 1% DC drop can be achieved at the package level.

III. Package and Assembly Process Description

The overall package is a 42.5mm square lidded BGA package. The BGA array is a full array on a 1.0mm pitch with A1 ball missing for orientation detection. The lid used is two-piece where the first piece is a flat Ni-plated copper pedestal or stiffener with a window to allow for the die and decoupling capacitors to be placed on the substrate. The second piece is a flat square placed over top of the die and the first piece of the lid. The 2nd-metal lid also acts as a heat spreader. The result is a lid construction of same overall dimensions of the package. The stiffener is attached to the laminate, and the heat-spreader is attached to the stiffener using an appropriate epoxy material. A high-performance material was used as the Thermal Interface Material (TIM) between the die and the lid with a thermal conductivity of ~3.6 W/m-K. We carried out reliability evaluation of the TIM using a laminate package with a specially designed thermal die. Summary of the performance of the advanced TIM in a FC-PBGA package will be summarized in the thermal reliability section V.

The laminate is a 400 micron thin-core 4-2-4 build up using Hitachi Chemical's E679 core material and Ajinomoto's GX13 build up material. The design rules used for the laminate incorporate a 100 micron nominal solder-mask defined (SMD) flip-chip pad on a 130 micron metal pad on a 200 micron pitch. This pad structure allows for escape routing in build-up layer one using a 20/20 micron line/space geometry.

The die is a 14.7mm square testsite fabricated using a 90nm low-K process in the "thin" wiring layers. It supports a total of 4699 Pb-free bumps on a 200 micron minimum pitch. The bump structure consists of a 110 micron diameter UBM with a plated Sn/Ag Pb-Free bump. The reflowed bumps are nominally 90 microns in height with a +/- 15 micron coplanarity requirement. A top-down view of the die with the bump-array is shown in Fig. 3A.

The PBGA packages were assembled using the process flow shown in Figure 3B. This is an abbreviated flow indicating major manufacturing steps. The test vehicle used also incorporated surface mounted capacitors. The SMT components are placed along with the flip chip die and reflowed together. An aqueous clean flux is used in the flip chip attach process, so there is an aqueous clean step following flip chip attach.

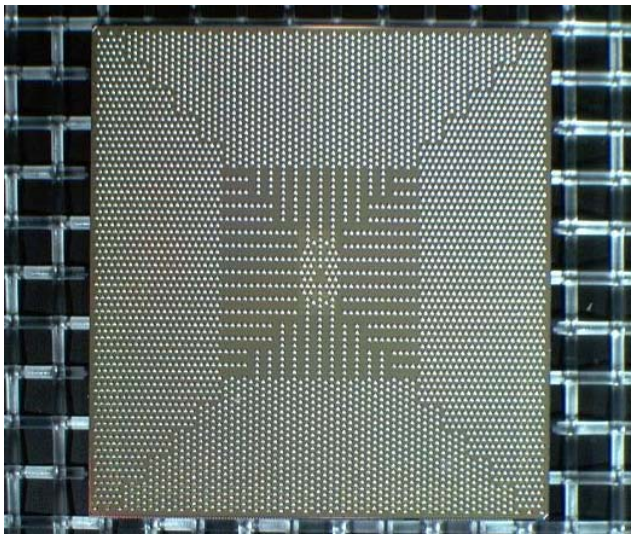

Fig. 3A: Test die showing 200 micron pitch bumps

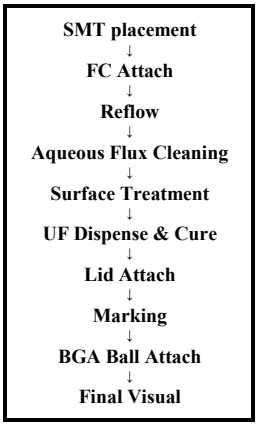

Fig.3B. Bond & assembly process flow for FC-PBGA

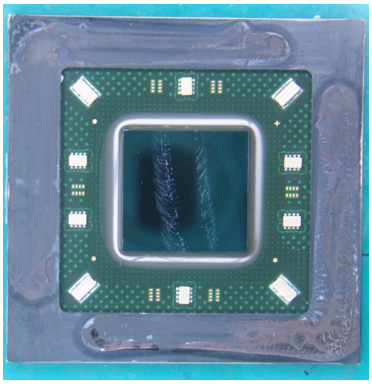

Fig 3C. Optical view of package top-surface with die and capacitors and stiffener (after lid removal)

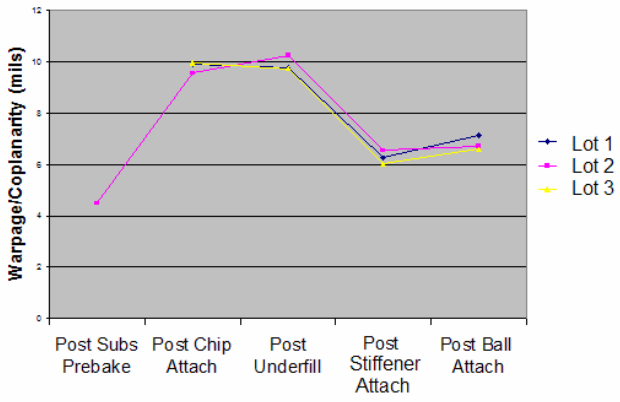

Fig 3D: Thin-core package warpage at various stages of assembly process.

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An optical micrograph of the package after die and SMT attach, underfill dispense and cure, and stiffener attach is shown in Fig 3C (with the lid removed). As can be seen, six multi-terminal low-inductance capacitors (MTLIC), and four two-terminal low-inductance ceramic capacitors were used in the test package.

Although there is extensive experience for flip chip on thicker 800 micron core organic laminates, the experience base building with thinner 400 micron core laminates is quite limited. One of the potential issues to consider is the level of package warpage resulting from the less stiff substrate. During the course of the build, the package warpage and final BGA coplanarity were monitored to ensure that the JEDEC 8mil (~ 203 micron) coplanarity criteria could be achieved. We were able to meet the BGA coplanarity despite the fact that the 400 micron thin-core build-up laminates were used. As can be seen in Fig 3D, the thin-core laminates can deform significantly after die attach due to the large CTE mismatch between die and laminate, and is brought down to below 8 mil or ~ 200 microns only after stiffener and lid attach.

One of the key challenges in reliability of flip-chip die with low-k wiring is the optimization of underfill used to lower the stresses on both the low-k wiring layers and the bump. It is generally known that the key issues for a good underfill are the following: good adhesion to both the die passivation and laminate solder resist layer, low CTE 1 (<Tg), and optimum Tg and Young's modulus. It is known from modeling (see for example reference 6) that low Tg (below ~100C), and low modulus are desirable to lower stress on the low-k die. On the other hand, high Tg (above~110C) and modulus are good for lowering strain on the bump. These two opposing requirements have to be balanced to achieve a reliable FC-PBGA package with a low-K die, and Pb-free bumps. We evaluated four different underfills from three suppliers in an initial assessment using Jedec L3 preconditioning and DTC testing (Deep Thermal Cycle). They had Tg in the range of 80-135C, and modulus in the range of 8-11GPa. There were no issues with underfill adhesion or voiding after underfill apply and cure with any of the underfills after preconditioning. However, only one underfill with Tg in the range of 100-110C, and modulus in the range of 9-10 GPa survived 1000 cycles of DTC without any bump or low-k die related fails. This underfill was selected for qualification module build and stressing.

IV. Reliability Stressing and Results

The package design ground rules that were evaluated with the 90nm low-K device are listed below ;

- Package 42.5mm sq. size, 2 pcs lid structure
- BGA ball : 1680 count, 1mm pitch, Sn/3Ag/0.5Cu
- Bump(C4) : 4699 count, diameter 100um on 200um pitch, plated SnAg
- Laminate minimum line width 20um, space 20um
- Laminate 2, 3 and 4 stack-via structures.

Reliability stresses and results are summrized in Table III: DTC, ATC (TCJ on card), HTS, THB, HAST, shock and vibration tests.

Stresses used and results at various stress readouts		Bump (C4)	BGA ball	Laminate via stack	Laminate nets
DTC (-55/125'C)	750cyc	0/45	0/45	0/45	0/45
	1000cyc	0/45	0/45	0/45	0/45
	1500cyc	0/45	0/45	0/45 [2]	0/45
	2000cyc	0/45	0/45	0/45 [2]	0/45
ATC on card (0/100'C)	1000cyc	0/45	0/45	0/45	0/45
	1500cyc	0/45	0/45	0/45	0/45
	3000cyc	0/45	0/45	0/45	0/45 [1]
	5000cyc	0/45	0/45	0/45	0/45 [1]
HTS (150'C)	1000hr	0/45	0/45	0/45	0/45
	2000hr	0/45	0/45	0/45	0/45
	3000hr	0/45	0/45	0/45	0/45
	4000hr	0/39	0/39	0/39	0/39
THB (85'C/85%RH/Bias)	1000hr	0/90	0/90	0/90	0/90
	1500hr	0/90	0/90	0/90	0/90
b-HAST (130'C/85%RH/bias)		0/45	0/45	0/45	0/45
Shock(100G, 200G)		0/21	0/21	0/21	0/21
Vibration		0/21	0/21	0/21	0/21

Notes [1)] : ATC card PTH plating cracks started from 3000cyc, but no package related fails observed.
[2)] : Laminate traces connected to 4-stack via may crack after 1000 DTC (see discussion in paper)

Table III: Reliability stress results

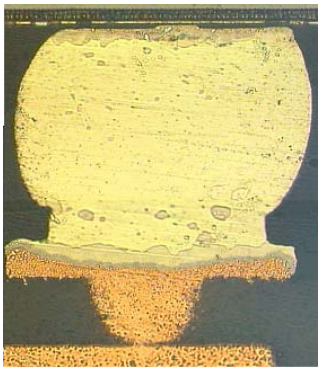

Fig.4A : Cross section of a bump after HTS 4000hrs

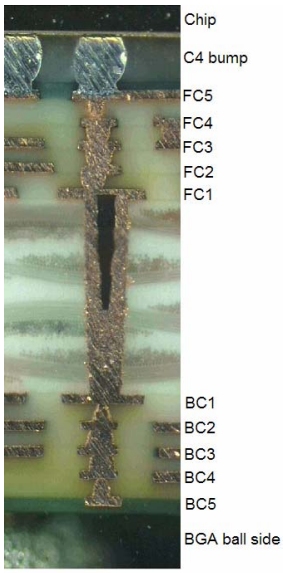

Fig.4B : Cross section of a laminate stacked-via after DTC 2000 cycles

Electrical test method was a 4 point measurement for bump joints, and 2 point measurement for BGA via chains, with a 10% resistance increase criteria for fails. A 3.3V +10% bias was applied for THB and HAST tests to monitor leakage

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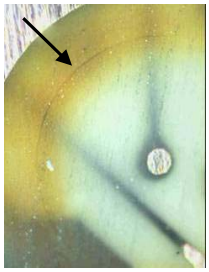
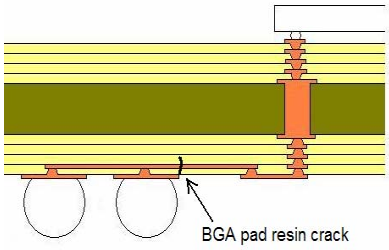
between other nets. Both electrical test, and post-test cross-sections confirmed no open or leakage failure of bumps, low-k die structure and laminate traces including stacked - vias, and BGA balls.

Fig.4A shows a cross section of a bump after HTS 4000hrs, Fig.4B is a cross section of a laminate stack-via after DTC 2000cycles. No cracks in bump or stack-vias were detected. Fig.4D shows cross sections after ATC 4000cycles. No cracks in bumps are seen, but small cracks in BGA balls are observed.

The only laminate fails identified were traces in the laminate build-up layer BC4 (the one above the BGA pad or BC5 layer). These traces are conneced to the 4-stack vias as shown in the schematic in Fig.4C(2). In this design, BGA pads had ~560micron solder resist openings. Around the BGA pad edge, resin layer could be cracked as shown in Fig. 4C(1), and the crack propagates to damage the trace underneath in the BC4 layer. It should also be noted that the resin cracking and the trace cracking in BC4 layer result from the severe mechanical stresses associated with the DTC stress. On card level ATC test, no resin cracking was seen up to 4000 cycles. As a result, depending on application conditions for particular products, design ground rules would restrict the use of 4-stack vias in the bottom build-up layers, or design the traces in the BC4 layer such that they are not in the areas of the die edges where the stresses in the laminate at BGA pad edges are high. Changing the BGA pad solder resist overcoat width is another solution. As shown in Fig.4E, 2x wider BGA pad soldermask overcoat delays the onset of resin crack/trace fails to higher DTC cycles. The overcoat width is defined as the length between solder resist opening on the BGA pad, and the edge of the BGA pad.

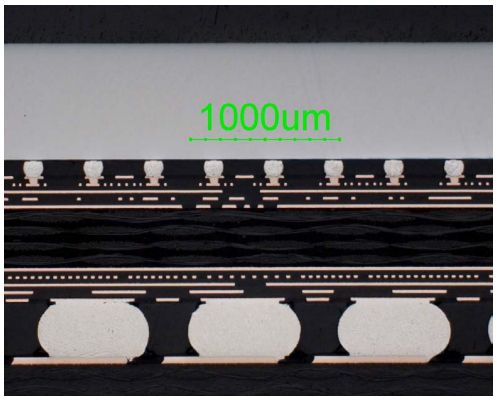


(1) Planer section BC4 layer view under BC5 BGA pad.

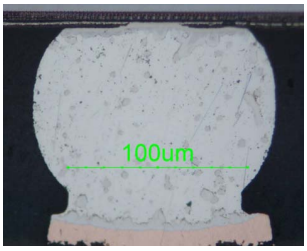


(2) Laminate cross section schematic of BGA pad crack location

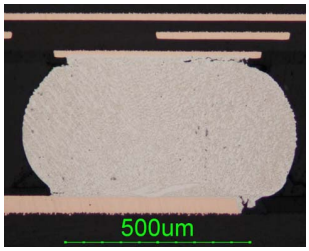
Fig.4C : BGA pad resin crack propagates to damage BC4 traces



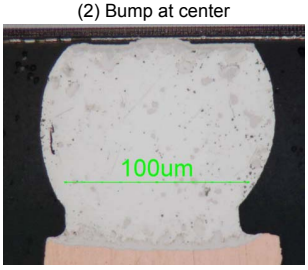
(1) Cross section at package center



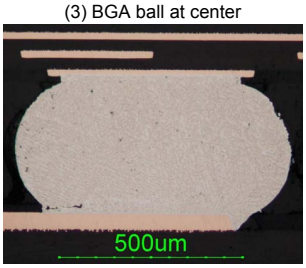
(2) Bump at center



(3) BGA ball at center



(4) Bump at chip edge



(5) BGA ball at chip edge

Fig.4D : Cross sections after ATC 4000 cycles

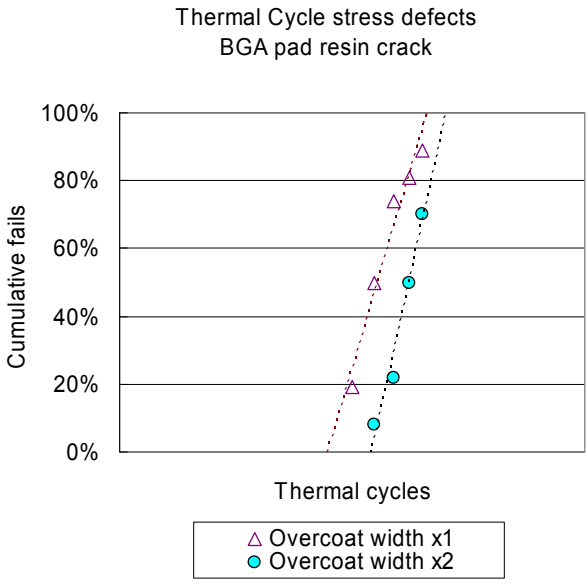


Fig.4E : BGA solder resist opening performance

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V. Thermal Reliability

One of the key requirements for the 90nm low-K technology is that thermal performance of the FC-PBGA package has to be significantly higher than 130nm devices. The goal of the qualification was to demonstrate that the package Rint of < 0.2C/W can be achieved after module assembly, and after typical stresses that are used for assessing the reliability of the thermal interface material (TIM) used between the die and the package lid. We used an advanced TIM with a thermal conductivity of ~3.6 W/m-K. The typical bondline achieved was in the 55-70 micron range. A special die (same size as the low-K die, and with Pb-free bumps) which has heaters and thermal sensors was used on a build-up PBGA package to carry out the thermal evaluation. The modules are tested for thermal measurements after module assembly, after JEDEC L-3 precon, and after DTC, T/H and HTS testing. The heaters on the die are used to heat up the die to a desired temperature, and die temperature (Tj) are measured using the on-chip thermal sensors, and the temperature of the lid at die center is measured through a thermocouple. The Rint values (also known as Theta-jc) are calculated from these measurements, and known material properties of the TIM and the package lid. The summary of the thermal test results are shown in Table IV. The data shown are for average of ten modules except for the time zero with multiple sensors readings in each module. The goal for 90nm FC-PBGA package was to achieve a Rint of 0.17C/W. As can be seen, a thermal performance much better than the requirement was achieved on a FC-PBGA package using an advanced TIM and assembly processes that assure a controlled bond line thickness. In addition, the TIM is stable through various reliability stresses typically used to evaluate thermal performance of a package.

Thermal data after various stresses	R_{int} (average) °C/W
Time zero (after preconditioning)	0.081
96hr HAST	0.083
HTS 1000hrs 125'C	0.085
THB 1000hrs 85'C/85%	0.089
DTC 1000cyc -55/125'C	0.078

Table IV: Summary of thermal reliability data.

VI. Discussion

Technology qualification of Pb-free bumps on a 90nm device technology with low-k wiring in the thin wiring levels has been achieved using a build-up laminate. In addition to Pb-free bumps, SAC-305 alloy was used for BGA connections, and Pb-free finish used on laminate joining pads for a Pb-free package. Reliability of Pb-free connections (bumps and BGA) was found to be excellent using standard stressess such as DTC, ATC, HTS, THB etc. Thin-core laminates (400 micron) with eight build-up layers with dense wiring rules can be used with Pb-free bumps and BGA. As discussed in section IV, resin cracking in DTC emanating from BGA pad edge is a concern, and package design ground rules should be optimized to prevent laminate trace carcking at or below 1000 DTC cycles. We found that underfill selection is key to achieve reliable low-k die and package performance in a Pb-free FC-PBGA package. Systematic evaluation of a series of underfills from suppliers are beneficial using representative die and laminate structures and sizes to select an optimum underfill material. Many 90nm devices with high power will require a lower package Rint to meet target Tj. Since thin-core packages will warp more than thick-core laminate packages after die attach, the package has to be designed with approriate stiifener/lid materials along with a high-conductivity TIM to achieve desired thermal performance.

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Note: As related to semiconductor products and materials, the term "lead free" does not mean that a product contains no lead. Rather, the term means that each homogeneous material of a product will likely have a maximum concentration value of 0.1% of lead by weight. The term "lead reduced" indicates that each homogeneous material of a product will likely have a maximum concentration value of 0.1% lead by weight, except those homogeneous materials where a RoHS Direction exemption may apply, such as an alloy containing >85% Pb, or a flip chip solder joint.

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